

Fast Digital Calibration of Static Phase Offset in Charge-Pump Phase-Locked Loops

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Abstract — Mismatches within the charge pump (CP) deteriorate the spectral performance of the CP-PLL output signal resulting in a static phase offset. Classical analog approaches to reducing this offset consume large silicon area and increase gate leakage mismatch. For ultra-deep-submicron (UDSM) technologies where gate leakage increases dramatically, reduction of static phase offset through digital calibration becomes more favorable. This paper presents a novel technique which digitally calibrates static phase offset down to < 10 ps for a PLL operating at 4.8 GHz, designed using a 1V 90nm CMOS process. Calibration is completed in only 2 steps, making the proposed technique suitable for systems requiring frequent switching such as frequency hopping systems commonly used in today’s wireless communication systems.

Keywords — Phase-locked loop (PLL), charge pump (CP) calibration, static phase offset.

I INTRODUCTION

Phase-Locked Loops (PLL) are important building blocks in modern wireless communication systems. Due to its superior acquisition ranges and reduced pull-in times [1], the charge-pump phase-locked loop (CP-PLL) is the most commonly implemented PLL architecture. A simplified block diagram of a CP-PLL is shown in Fig. 1.

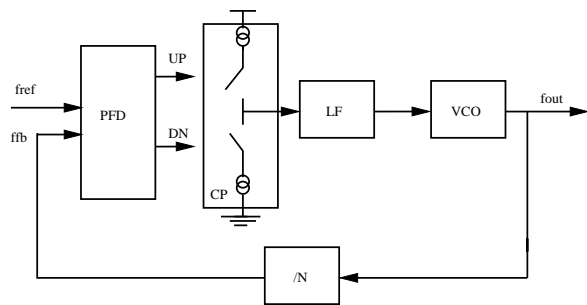


Fig. 1: CP-PLL Block Diagram

As seen in Fig. 1, the CP-PLL is a feedback system which produces a stable output frequency (f_{out}) from an input reference frequency (f_{ref}). Both frequencies are compared by a phase frequency detector (PFD) which produces output pulses proportional to the phase / frequency difference at the input to the PFD. These pulses are converted to analog signals by the charge-pump (CP) whose mean output is proportional to the initial phase / frequency difference. This mean is then extracted by the loop filter (LF) which outputs a control voltage for the voltage controlled oscillator (VCO). This control voltage forces the VCO to adjust its output frequency until it matches a multiple of the input reference frequency, the multiple being determined by the feedback divider ratio ($N = f_{out}/f_{ref}$). Once both frequencies are equal, the PLL is in lock.

While in lock, in order to avoid a dead zone of operation so that all input phase differences can

be tracked, the PFD transmits equal pulses of a specified duration (longer than the turn on time of the CP) to the CP. Provided both the UP and DN (down) networks of the CP match perfectly, these pulses do not affect the output frequency as no net change to the VCO frequency occurs. In reality however, mismatches occurring between the UP and DN networks gives rise to a mismatch current which alters the VCO frequency. This results in sidebands at an offset of $\pm f_{ref}$ of the PLL output frequency that deteriorate its spectral performance [2]. One approach to reducing these sidebands is by decreasing the PLL loop bandwidth. This is however not an optimal solution as it results in increased noise from other noise sources within the PLL such as the VCO [3]. A more efficient solution involves reducing the static phase offset itself.

In this paper we present a novel approach to reducing the static phase offset of a CP-PLL suitable to ultra-deep-submicron (UDSM) technologies. The paper is organised as follows. Section II details the sources of static phase offset in a CP-PLL. Related work is reviewed in Section III. The proposed technique and circuit implementation are presented in sections IV and V respectively. Simulation results are then presented in section VI with a final conclusion given in section VII.

II STATIC PHASE OFFSET

Specific sources of static phase offset are shown in Fig. 2.

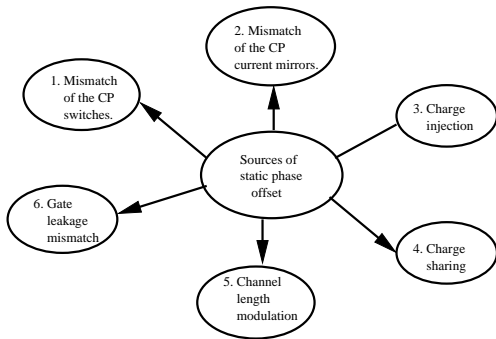


Fig. 2: Sources of static phase offset

Sources 1,2 and 4 correspond using a single ended CP architecture to the matching of different devices. Fully differential CP structures reduce this constraint to how well a PMOS matches a PMOS and an NMOS matches an NMOS [4], which is classically achieved by increasing device dimensions [5]. Static phase offset due to charge injection and charge sharing can then be further reduced with current steering [6]. However as charge sharing corresponds to the matching of peak currents occurring at the turn on instance of the CP switches, it is also dependent on channel length

modulation. The low voltage supplies which accompany UDSM technologies do not permit the reduction of channel length modulation through stacking, as this degrades the CP output voltage swing. Fortunately stacking need not be pursued as increasing device dimensions to reduce mismatch results in long channel devices exhibiting high output conductance's, hence providing more ideal current sources.

Although increasing device dimensions reduces sources 1 to 5, it is in direct contrast to static phase offset due to gate leakage mismatch. Gate leakage is a quantum mechanical effect and as such exhibits spread. The matching of this spread between devices is difficult, hence giving rise to gate leakage mismatch. As shown in [7], gate leakage mismatch increases with increasing device dimensions and so cannot be reduced using classical techniques. Furthermore as technologies scale down, gate oxide thickness must reduce to maintain constant scaling. This results in a drastic increase in gate leakage (and hence gate leakage mismatch) when migrating to lower technology nodes.

Therefore as the classical approach of reducing the sources of static phase offset increases gate leakage mismatch (in addition to consuming large silicon area), alternative techniques need to be researched for UDSM technologies where this source becomes increasingly influential.

With digital logic being correspondingly cheaper to implement on UDSM technologies, the concept of digitally assisted analog becomes attractive whereby the digital computational power of lower technology nodes is used to calibrate high performance CPs in order to overcome non-idealities. As such, the use of digital calibration techniques to reduce all sources of static phase offset (including gate leakage mismatch) becomes justifiable for UDSM technologies.

III RELATED WORK

Published calibration techniques focus on reducing static phase offset by reducing mismatch current using trim current sources. The main difference between current publications is the mechanism of determining the number of trim sources to be adjusted. In [8], this is done by detecting the static phase offset using a replica CP and adjusting the trim sources successively. The disadvantage of this approach is that it assumes perfect matching between the replica CP and the PLL-CP, an assumption invalid for UDSM technologies. In addition, the successive approach to adjusting the trim sources can result in prolonged calibration times. In [9], the static phase offset is detected at the PFD output using a bang-bang phase detector, again to adjust the trim sources successively. This approach has the advantage of not requiring

a replica CP but still suffers from prolonged calibration times due to the successive approach of adjusting the trim sources. A variation of this approach is then reported in [10] where the static phase offset is detected at the input to the PFD which is then calibrated down to a specified value.

The common feature of [8, 9, 10] is that only the static phase offset is detected hence necessitating a successive approach to adjusting the trim sources. This results in prolonged calibration times as n steps are potentially required, n being the number of trim current sources. Calibration time is in addition to PLL locking time and so should be reduced for systems requiring frequent switching, such as frequency hopping systems commonly used in today's wireless communication systems.

A potentially faster approach is pursued in [11], where the number of trim sources is digitally computed based on voltage measurements taken at the LF. Although this approach only requires 2 steps, it still exhibits prolonged calibration times due to the length of time required to make the LF measurements. In addition, comparators are used in the calibration loop which are not optimal for UDSM technologies where input offset voltages may compromise calibration resolution.

IV FAST DIGITAL CALIBRATION OF STATIC PHASE OFFSET

The proposed technique reduces the static phase offset by measuring it at the PFD input during lock. Using this measurement the number of trim sources required to minimise the resulting mismatch current are computed, thereby eliminating the need for a successive approach and associated prolonged calibration times. As the calibration loop consists of purely digital blocks, it achieves fast calibration well suited to UDSM technologies.

The proposed calibration technique is achieved in two steps. The first step measures the static phase offset and adjusts the required number of trim sources; the second step involves a re-measurement of the offset to quantify any residual error arising from inaccuracies in the measurements of the first step and trim source magnitudes. A block diagram for the proposed system is shown in Fig. 3.

As shown in Fig. 3, a lock detect circuit (LD) enables the calibration loop when the PLL has locked. Once enabled, the calibration loop measures the static phase offset using a Time-to-Digital Converter (TDC). The output of the TDC is then processed by a digital control block to determine the number of trim current sources to be adjusted.

The TDC measures the offset by directly measuring the difference in arrival times between the reference and feedback pulses when the PLL is in

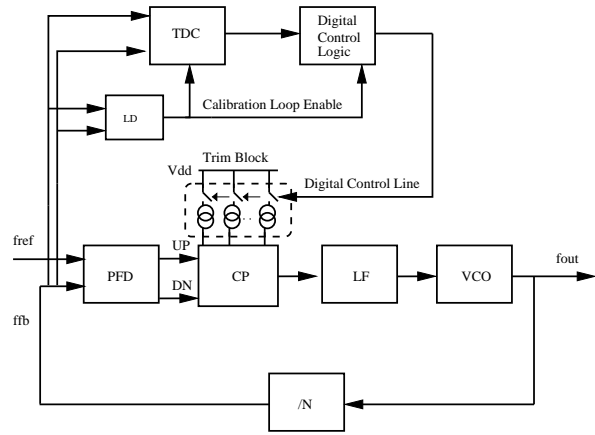


Fig. 3: Block diagram of the proposed calibration system

lock. Using this information, the digital control block calculates how many trim sources need to be adjusted to minimise the mismatch current and resulting static phase offset. From this it generates a thermometer code which is sent to the trim block to switch in the required number of trim sources.

Assuming the mismatch current flows only for the duration of the PFD steady state pulse, static phase offset can be defined as:

$$|\phi_e| = 2\pi \frac{\Delta t_{PFD}}{T_{ref}} \frac{\Delta i_{cp}}{I_{cp}} \quad (1)$$

where mismatch current between the UP and DN networks, overall CP current, PFD steady state pulse duration and reference period are represented by Δi_{cp} , I_{cp} , Δt_{pfd} and T_{ref} respectively. This results in an offset defined by:

$$t_{offset} = \frac{|\phi_e|}{\omega_{ref}} = \frac{\Delta t_{pfd} \Delta i_{cp}}{I_{cp}} \quad (2)$$

where reference frequency is represented by ω_{ref} .

The number of current sources required to compensate this offset is defined as:

$$M = \frac{t_{offset}}{t_{res}} \quad (3)$$

where t_{res} is the resolution of the calibration loop i.e. the offset produced from switching in one single trim source.

Taking an example to illustrate this: Assume $\Delta t_{pfd} = 1$ ns, $I_{cp} = 100$ μ A, $F_{ref} = 20$ MHz and $\Delta i_{cp} = 8$ μ A (8% current mismatch). From (1), this current mismatch will result in a static phase offset of 10 mrad, which from (2) gives an offset of 80 ps. Assuming each trim source provides a nominal current of 1 μ A, again from (2) it can be seen that the switching in of one single trim source will result in a offset of 10 ps. Therefore, from (3), a total of 8 trim sources is needed to compensate

for the static phase offset caused by the initial 8 % current mismatch.

The above described step must be repeated to account for any residual errors arising from inaccuracies in the TDC measurements and trim source magnitudes. Therefore calibration is complete after only two steps, with its digital nature achieving short calibration times which do not present significant overhead to the overall PLL settling time or interfere with the PLL loop dynamics.

V CIRCUIT DESCRIPTION

To verify the proposed technique, a PLL with fast digital calibration of static phase offset was designed for a 1P9M 90nm CMOS process, with reference and VCO center frequencies set to 20 MHz and 4.8 GHz respectively.

a) Standard Blocks

A standard PFD was used exhibiting a delay time of 1 ns (shown by simulation to be sufficiently longer than the worst case turn on time of the CP switches). A differential CP is employed due to its ability in reducing sources 1 to 4 of Fig. 2 down to an issue of how well NMOS matches NMOS and PMOS matches PMOS, in addition to doubling the output voltage swing and reducing low frequency common mode noise [4]. The simulated CP is taken from [12] as it uses current steering, with I_{cp} set to 100 μ A. A 2nd-order LF is used with pole and zero positions set to 2.6 and 0.4 times the 200 kHz loop bandwidth to achieve a phase margin of 49°. The VCO is modeled to exhibit a gain of 30 MHz/V with the integer feedback divider constant set to 240 to provide the required output frequency from the input reference frequency.

b) Time-to-Digital Converter (TDC)

The TDC is responsible for measuring the static phase offset and so its resolution determines the minimum offset achievable. Improved resolution can be achieved by increasing the number of delay stages in the TDC. However, classical TDCs suffer from non-linearity due to mismatch between delay stages which becomes a major limitation for UDSM technologies where mismatch increases. To address this issue, the gated ring oscillator architecture described in [13] was used whose block diagram is shown in figure 4.

The gated ring oscillator consists of a classic n -stage inverter based oscillator with switches placed in series with the positive and negative power supply connections of each inverter. This enables the oscillator to run during a defined interval with its state at the end of each interval being held. Oscillator transitions occurring during each measurement interval are then counted and summed to give a measurement of the static phase offset. The ad-

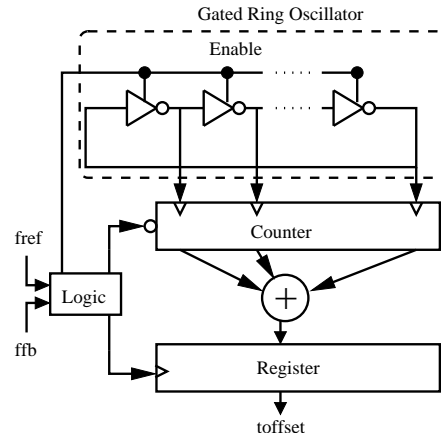


Fig. 4: Block diagram of TDC

vantage of this approach is that the segments of oscillator used per measurement interval are data weighted to achieve a first order shaping of the mismatch error.

The TDC was designed with 21 stages to achieve a resolution of < 10 ps.

c) Lock Detect (LD), Digital Control Logic and Trim Block

The Lock Detect and Digital Control Logic blocks are standard digital blocks. Lock Detect was designed with the Digital Control Blocks being implemented in Verilog and synthesized using Mentor Graphics synthesis tools.

The Trim Block consist of 32 identical trim current sources applied to both the UP and DN branches of the CP to give a total current adjustment range of ± 32 %. These current sources are controlled by the Digital Control Logic block where each source switches in a nominal current of 1 μ A (1 % of I_{cp}). Such a small current change guarantees the PLL will not come out of lock during calibration. As the matching of these current sources is important, they are laid out as unit sources in a common-centroid pattern to minimize mismatch over process, voltage and temperature variation. To further improve on matching, a data weighted average technique is employed, whereby successive groups of trim sources are sequentially shifted through the block to average out the mismatch [14].

VI SIMULATION RESULTS

To verify the proposed technique, the described circuit was simulated for the case when PLL is in lock. The workings of the calibration can be seen in Fig. 5 which plots the UP and DN steady state pulse widths from the PFD against time, where the static phase offset is represented by the difference between the pulse widths. Included at the bottom of the plot is the thermometer code generated by

the digital control block to switch in the required number of current sources.

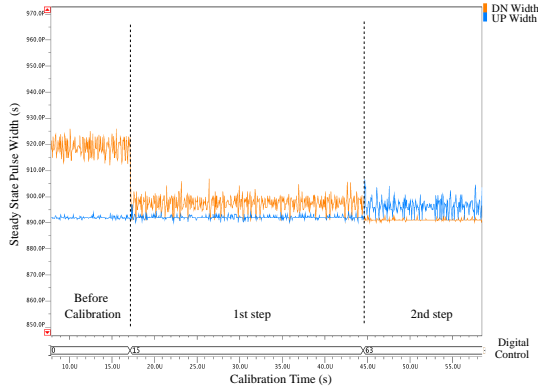


Fig. 5: Simulation of calibration scheme

In Fig. 5, the UP current is initially $103 \mu\text{A}$ and DN current is $100 \mu\text{A}$ to give a difference in pulse widths of $\approx 30 \text{ ps}$. In other words an offset of $\approx 30 \text{ ps}$ at the input to the PFD has resulted from the 3 % current mismatch as in agreement with (2). The trim sources provide a nominal $1 \mu\text{A}$, where the first step switches 4 sources in parallel to the DN current. Due to inaccuracies in the TDC measurements and trim current magnitudes, the difference in pulse widths is still greater than the TDC resolution (10 ps) after the first step. This necessitates the second step which switches in an additional 2 sources. This succeeds in reducing the difference in pulse widths to below 10 ps meaning that the static phase offset has been reduced to below 10 ps . Calibration is complete after the second step where the static phase offset has been minimised.

The worst case contributions of the sources of static phase offset described in section II, on the simulated circuit are shown in Table 1.

Source	t_{offset} (ps)
1,2,6	97 (62%)
5	53 (34%)
3,4	6 (4%)

Table 1: Contributions to static phase error

From Table 1, the CP is shown to exhibit a worst case offset of 156 ps . Reducing this offset down to 10 ps thus requires 16 trim current sources, although 32 are used because of the data weighted averaging. This leads to a total silicon area consumption for both the CP and corresponding calibration circuitry of $520 \mu\text{m}^2$. As device mismatch is inversely proportional to the square root of

area [5], the classical approach to achieving a reduction in this static phase offset would correspond to an increase in the matching critical transistor areas by a factor of 256. This represents a substantial increase in silicon area which, for UDSM technologies, would not minimise the static phase offset due to the increase in gate leakage mismatch.

A final performance summary of the proposed calibration technique is shown in Table 2.

Technology	90nm CMOS
Power Supply	1V
I_{cp}	$100 \mu\text{A}$
ϕ_e	$< 1.2 \text{ mrad}$
t_{offset}	$< 10 \text{ ps}$
Calibration steps	2
Area	$520 \mu\text{m}^2$

Table 2: Performance Summary

VII CONCLUSION

The reduction of static phase offset using classical analog techniques consumes large silicon area in addition to increasing gate leakage mismatch. As such, digital calibration becomes more favorable for UDSM technologies. This paper presented a novel technique for digitally calibrating the static phase offset of a CP-PLL. By measuring the static phase offset, the number of current sources required to minimise the offset are computed, enabling calibration to be completed in 2 steps. The technique was verified for a 4.8 GHz PLL, designed using a 1V 90nm CMOS process which achieves a reduction of the static phase offset to below 10 ps (the resolution of the loop). The CP and corresponding calibration circuitry occupy only $520 \mu\text{m}^2$, representing substantial savings in silicon area over classical analog approaches to reducing the offset. The calibration loop is completely digital making it well suited for UDSM technologies where the 2 step calibration approach enables fast settling times, suitable for systems requiring frequent switching such as frequency hopping systems commonly used in today's wireless communication systems.

VIII ACKNOWLEDGMENT

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